DM7045

100BASE-Tx Small Form Factor Pluggable Module

Product Requirements Ver 2.0

2/5/15

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0.2 CONTENTS

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1 INTRODUCTION

The scope of this document is to specify the technical details for a "Hot-Pluggable" 100Base-TX Ethernet electrical interface SFP module.

The SFP 100Base-TX Electrical module (referred to as "100Base-TX SFP" or just "SFP" in the rest of this document) shall comply with the requirements of the IEEE802.3 (**see [2]**) for the front-end interface and the SFP MSA (**see [1]**) for physical form and host board interface unless otherwise stated in this document.

The SFP is to mimic being an optical module for use with a PHY operating in 100Base-FX mode. It is to convert the 100Base-FX LVPECL signalling from the PHY connection into a 100Base-TX compatible format.

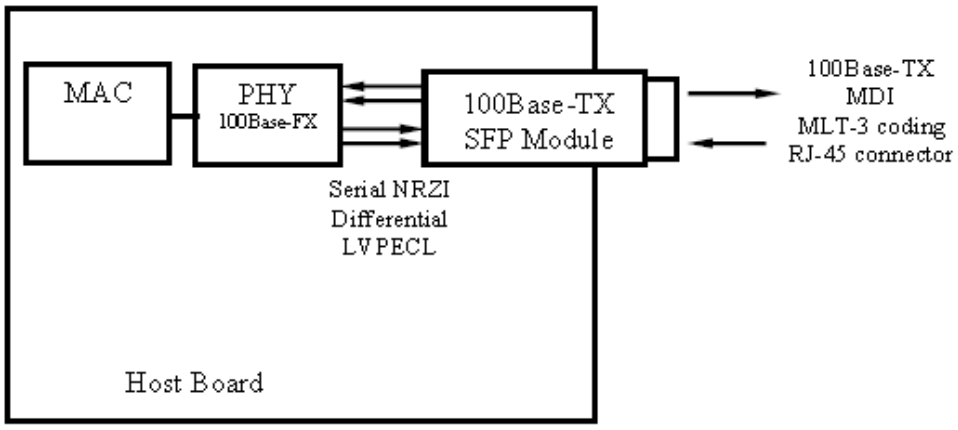

Figure 1-1 – 100Base-TX SFP Data Interfaces.

End of section

2 FUNCTIONALITY

2.1 DATA ENCODING AND DECODING

A summary of the module's functionality is as follows:

- Convert a NRZI, serial differential data stream from the host board into MLT-3 encoded data.
- Drive the MLT-3 encoded data out as a, 100Base-TX compliant interface.
- Convert the received MLT-3 signal into a NRZI, serial, differential data stream.
- Perform any necessary scrambling / descrambling between the 100Base-TX and 100Base-FX formats.

The SFP shall be capable of encoding and decoding of data simultaneously to provide full duplex operation. Half duplex operation shall also be supported.

The MLT-3 line coding shall be presented on the RJ-45 interface as a 100Base-TX compliant device.

2.2 AUTO NEGOTIATION

This device is configured for Forced 100Mbps with Auto-negotiation for Full or Half Duplex and pause ability.

2.2.1 Parallel Detection

Parallel detection of the MDI cable data speed applied to the SFP MDI interface, normally in conjunction with auto-negotiation, is not required.

2.3 AUTO MDIX

The SFP shall support automatic MDIX, namely, the swapping of Rx and Tx pairs on the 100Base-TX interface to match a 'straight-through' or 'crossed' cable connection based on sensed signals.

End of section

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3 ELECTRICAL CHARACTERISTICS

3.1 MAXIMUM RATINGS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Absolute Operating Temperature Range (1)	-	-40	-	+85	°C
Storage Temperature Range (2)	-	-40	-	+125	°C
Supply Voltage	VccT, VccR	0	-	3.8	V
Input Data Signal Levels (AC coupled)	TD+, TD-	-	-	3	V
Relative Humidity	RH	-	-	85	%
Static Discharge Voltage (human body)	ESD	-	-	500	V
Lightning Strike (RJ-45 Screen)		-	-	2000	V

NOTES:

(1) Case temperature range for operation without 100Base-TX SFP Module damage
(2) Temperature range for storage without 100Base-TX SFP Module damage

Table 3-1 100Base-TX SFP Maximum Absolute Ratings

3.2 OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Case Temperature Range (1)	-	-40	-	+85	°C
Supply Voltage	VccT, VccR	3.135	3.3	3.465	V
	Icc	-	-	0.3	A
Power Dissipation	-	-	0.8	1	W

NOTE:
(1) Case temperature range in which the 100Base-TX SFP Module performs within the required specifications.

Table 3-2 100Base-TX Operation Conditions

3.3 CONNECTOR AND PIN ASSIGNMENT

Please refer to SFP MSA, (see [1]), for SFP Connector and Pin assignment details and associated notes. The specific details of the 100Base-TX SFP Connector and Pin assignment will be detailed here:

3.3.1 Pin Assignment

Pin Number	Name	Function	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	Common with Receiver Ground
2	Tx Fault	Transmitter Fault Indicator	3	Not Supported, pull low. See section 3.5.1
3	Tx Disable	Transmitter Disable	3	Transmitter disable on High or Open. See section 3.5.4
4	MOD-DEF2	Module definition 2	3	Data line for serial ID
5	MOD-DEF1	Module definition 1	3	Clock Line for Serial ID
6	MOD-DEF0	Module definition 1	3	Ground within Module
7	Rate select	Select between Full or Reduced bandwidth mode	3	See section 3.5.5
8	LOS	Loss Of Signal	3	Loss Of Signal – See section 3.5.3
9	VeeR	Receiver Ground	1	Common with Transmitter Ground
10	VeeR	Receiver Ground	1	Common with Transmitter Ground
11	VeeR	Receiver Ground	1	Common with Transmitter Ground
12	RD-	Receiver Inverted DATA out	3	AC coupled
13	RD+	Receiver Non-Inverted DATA out	3	AC coupled
14	VeeR	Receiver Ground	1	Common with Transmitter Ground
15	VccR	Receiver Power	2	Common with Transmitter Power
16	VccT	Transmitter Power	2	Common with Receiver Power
17	VeeT	Transmitter Ground	1	Common with Receiver Ground
18	TD+	Transmitter Non-Inverted DATA in	3	AC Coupled with 100R Termination
19	TD-	Transmitter Inverted DATA in	3	AC Coupled with 100R Termination
20	VeeT	Transmitter Ground	1	Common with Receiver Ground

Table 3-3 100Base-TX SFP Pin Assignment.

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3.3.2 Connector Arrangement

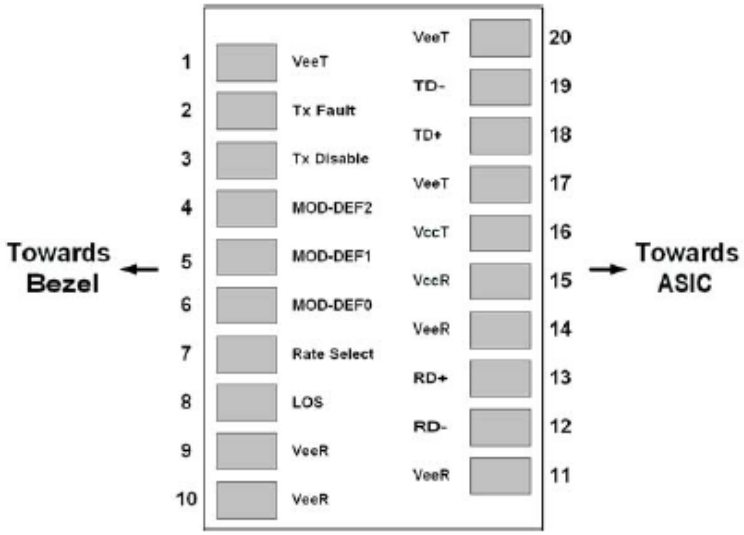

Figure 3-1 100Base-TX SFP Connector Arrangement.

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3.4 DC POWER SUPPLY

The power supply shall meet the requirements of SFP MSA (see **[1]**) and also the values shown in Table 3-4.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Voltage (1)	VccT & VccR	+3.125	+3.300	+3.465	V
Power Supply Current (Steady State)	Icc	-	-	0.3	A
Inrush Current greater then Steady State (When hot plugging occurs) (2)	Icc	-	-	0.03	A
Power consumption	-	-	-	1	W

Notes:

(1) Please refer to Figure 3-2 for power filter configuration.
(2) When power supply is using the filter configuration of Figure 3-2.

Table 3-4 100Base-TX SFP Power Requirements.

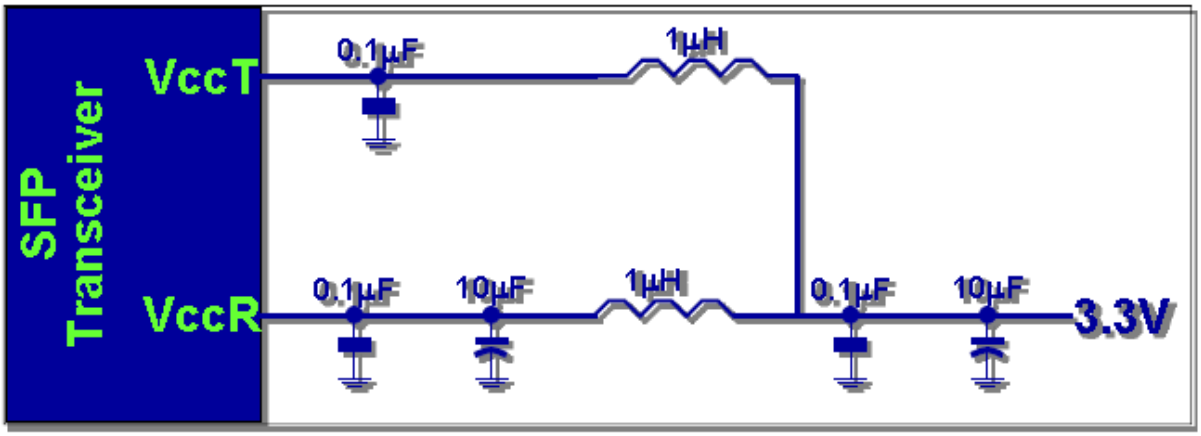

Figure 3-2 Power Supply Filtering Configuration. (Provided on the Host Board).

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3.5.1 Host Board Electrical Interface Voltage Characteristics

Table 3-5 details Transmitter interface characteristics and **Table 3-6** details the receiver interface characteristics.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Data Signal Levels (AC coupled) (1)(2)	TD+ and TD-	0.5	-	2.4	V
Transmitter Fault indication (3)	Tx Fault	0		0.8	V

NOTES:

(1) These are differential Inputs.
(2) Differential inputs are AC coupled and terminated with 100R differential terminations inside the 100Base-TX SFP.
(3) Tx Fault in this application is permanently tied to logic '0'.

Table 3-5 Transmitter Voltage Characteristics

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Output Data Signal levels (AC Coupled) (1)(2)		RD+ and RD-	0.65	-	2.000	V
Loss Of Signal (3)	High – LOS	LOS	2.000	-	VccR+0.3	V
	Low – Normal		0	-	0.800	
Transmit Disable (4)	High – Tx Disabled	TX_DIS	2.000	-	VccT+0.3	V
	Low – Tx Enabled		0	-	0.800	

NOTES:

(1) These are differential outputs.
(2) Differential outputs are AC coupled inside the 100Base-TX - SFP and terminated with 100R differential terminations on the host board.
(3) When used with a 4k7 – 10k pull-up resistor to +3.3v on the Host Card.
(4) A 4k7 – 10kpull-up resistor is inside the SFP module.

Table 3-6 Receiver Voltage Characteristics

3.5.2 Host Board Electrical Interface Timing Characteristics

The host board interface timing characteristics are as defined in the SFP MSA, (see **[1] section B3).** Due to the non-optical nature of the 100Base-TX module, most of the timing parameters do not apply. The parameters that do apply are shown below.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Serial ID Clock Rate	f_serial_clk	-	-	100	kHz

Table 3-7 Control and Status Interface Timing

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3.5.3 LOS Condition

LOS is an open collector/drain output, which should be pulled up with a 4.7K – 10KOhm resistor on the host board. The pull up voltage shall be between 2.0V and VccT/R.

This signal is tied LOW in the SFP.

3.5.4 Transmit Disable

Transmit Disable (TX_DIS) is a control signal from the host system to the SFP module with a 4.7K – 10KOhm pull-up resistor in the SFP module itself. When TX_DIS is in a logic low state the module shall perform as normal. When set to a logic high state, the MDI transmitter interface shall be disabled. This includes the outputs when the module has switched to a MDIX mode

3.5.5 Rate Select

Rate Select (RATE_SEL) is a control signal from the host system to the SFP module. It is not implemented in the SFP module. It is pulled down with a 33K ohm resistor.

3.6 100BASE-TX MDI ELECTRICAL INTERFACE

The transmit and receive interfaces shall be conformant with clause 25 of (see [2]). Note that most of that section refers out to section 8.1 and 8.2 of References, with some modifications. A brief overview of parameters is shown in this section.

3.6.1 Transmitter Interface

The MDI transmitter interface shall have the following properties when driven directly into a 100Ohm load

Characteristic	Minimum	Maximum	Units
Differential Signal	950	1050	mV peak
Amplitude Symmetry	98	102	%
Rise and Fall time	3	5	ns
Rise and Fall time symmetry	0	0.5	ns
Duty Cycle Distortion (peak to peak)	0	0.5	ns
Transmit Jitter	0	1.4	ns
Overshoot	0	5	%

Table 3-8 Transmitter Interface Characteristics

For more details, see reference (**[2]**).

The SFP module will be presented with data from the host system for transmission with jitter up to the Ethernet limits. The SFP module shall not add any further jitter to this signal for transmission.

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3.6.1.1 Return Loss

The differential impedance shall be such that the return loss is greater than 16dB from 2MHz to 30MHz, greater than (16-20log(f/30MHz))dB from 30MHz to 60MHz, and greater than 10dB from 60MHz to 80MHz. The requirement is specified for any reflection due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range of 85Ohms to 111Ohms. The return loss shall be maintained when the receiver circuit is powered.

Frequency	Specification
2MHz	16dB
30MHz	16dB
60MHz	10dB
80MHz	10dB

Table 3-9 100Base-TX Receive Return Loss

Frequency	Specification
2MHz	16dB
30MHz	16dB
60MHz	10dB
80MHz	10dB

Table 3-10 100Base-TX Transmit Return Loss

3.6.2 Receiver Interface

The receiver interface is to be sensitive enough to decode error-free data from a worst case specified transmitter over at least 100m of CAT-5 cable.

3.6.3 Physical Connections

The MDI interface will utilise a RJ-45 connector and the following connections:

Contact	Normal Signal
1	Transmit +
2	Transmit -
3	Receive +
4	
5	
6	Receive -
7	
8	

Table 3-11 RJ-45 Connection

Additional circuitry can be connected to the unlabeled pins to reduce EMC emissions and susceptibility.

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3.7 CONTROL AND DATA INTERFACE

100Base-TX SFP Module shall provide a serial communications interface between the Host board controlling device (typically a microprocessor) and the 100Base-TX SFP Module. This shall be exclusively realised by means of two-wire digital interface as stated in the SFP MSA, (see **[1]).**

Any two-wire implementation shall not use any "clock stretching" techniques from the SFP module.

The 100Base-TX SFP Module shall have an EEPROM that will contain data that describes the module's capabilities, interfaces, manufacturer and other information, refer to the SFP MSA, (see **[1]).**

The memory map is summarised here:

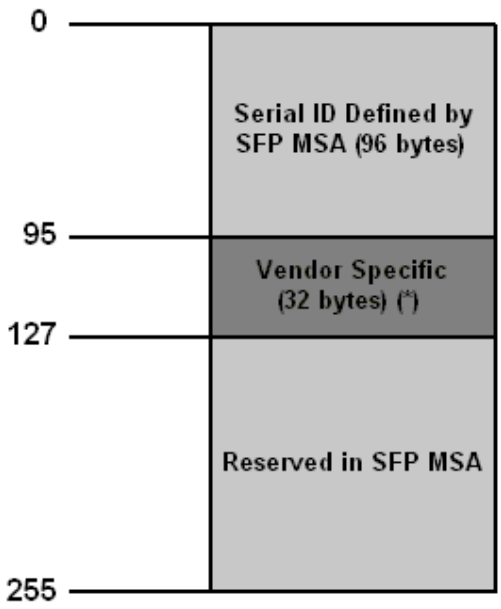

Figure 3-3 100Base-TX SFP EEPROM map

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3.7.1 Serial ID EEPROM map

The module identification is located in the EEPROM, which is accessed over the 2-wire serial management interface. The address of the EEPROM is 0xA0 (1010000X). Table 3-12 shows the SFP EEPROM memory map and the actual data.

Data Address	Field Size	Field Name	Field Description	Field Value	Value Description
BASE ID FIELDS					
0	1	Identifier	Type of serial transceiver	03	SFP TRANSCEIVER
1	1	Ext. Identifier	Extended identifier of type of serial transceiver	04	WITH SERIAL ID
2	1	Connector	Code for connector type	00	UNSPECIFIED
3-10	8	Transceiver	Code for electronic or optical compatibility	00,00,00,00, 00,00,00,00	
11	1	Encoding	Code for serial encoding algorithm	01	8B10B ENCODING
12	1	BR, Nominal	Nominal bit rate, units of 100Mbits/sec	01	125 MBPS
13	1	Reserved		00	RESERVED
14	1	Length(9m) – km	Link length supported for 9/125 mm fiber, units of km	00	NA
15	1	Length (9m)	Link length supported for 9/125 mm fiber, units of 100m	00	NA
16	1	Length (50m)	Link length supported for 50/125 mm fiber, units of 10m	00	NA
17	1	Length (62.5m)	Link length supported for 62.5/125 mm fiber,units of 10m	00	NA
18	1	Length (Copper)	Link length supported for copper, units of meters	64	100 METERS
19	1	RESERVED		00	RESERVED
20-35	16	Vendor name	SFP transceiver vendor name (ASCII)	4D,45,54,48, 4F,44,45,20, 45,4C,45,43, 20,20,20,20	METHODE ELEC (ASCII)
36	1	Reserved		00	RESERVED
37-39	3	Vendor OUI	SFP transceiver vendor IEEE company ID	00,17,05	METHODE OUI
40-55	16	Vendor PN	Part number provided by SFP transceiver vendor (ASCII)	44,4D,37,30, 34,35,20,20, 20,20,20,20, 20,20,20,20	DM7045 (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)	2D,20,20,20	
60-62	3	Reserved		00,00,00	RESERVED
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)	VARIES	
EXTENDED ID FIELDS					
64-65	2	Options	Indicates which optional SFP signals are implemented	00,10	TX DISABLE IMPLIMENTED
66	1	BR, max	Upper bit rate margin, units of %	00	
67	1	BR, min	Lower bit rate margin, units of %	00	
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)	VARIES	VENDOR SERIAL NUMBER
84-91	8	Date code	Vendor's manufacturing date code	VARIES	YY-MM-DD-LOT#
92-94	3	Reserved		00,00,00	
95	1	CC_EXT	Check code for the Extended ID Fields (addr. 64 to 94)	VARIES	
VENDOR SPECIFIC ID FIELDS					
96-127	32	Read-only	Vendor specific data	ALL FF	

Table 3-12 EEPROM Memory Map and Contents

3.7.2 Phy Register Access

The DM7045 transceiver supports access to the PHY Registers over the 2-wire serial interface. The registers may be accessed at address BE/BF (READ/WRITE). The register set includes standard interface registers per IEEE802.3 Clause 22. In addition, the register set can be used to configure the device for special modes of operation. Note: Improper use of PHY register access can result in the abnormal behavior of the device.

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4 MECHANICAL REQUIREMENTS

All plastics within the 100Base-TX SFP Module must be UL94V-0 rated.

The 100Base-TX SFP will have a RJ-45 connector instead of an SFP optical interface.

4.1 MECHANICAL DIMENSIONS

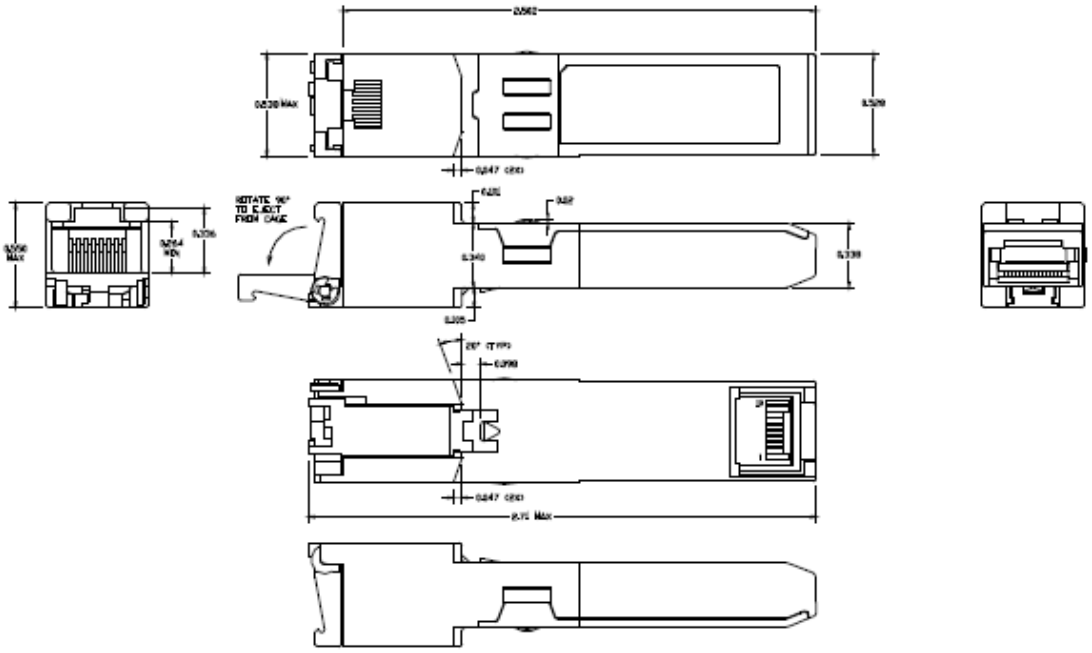

Figure 4-1 100Base-TX SFP Module package mechanical dimensions

4.2 100BASE-TX SFP HOST PCB ELECTRICAL CONNECTION

The 100Base-TX SFP Host Board Connector and the related pin assignment shall be realised in full compliance with the indications stated in the SFP MSA, **(see [1])**. The pin mapping is illustrated for ease of understanding in **Figure** 4-2, while **Table 3-3** details the description and meanings of each pin. Please note that this is an indicative picture only, whilst a detailed drawing is illustrated in **Figure 4-3.** Please refer to the SFP MSA for mechanical details, (see **[1]**).

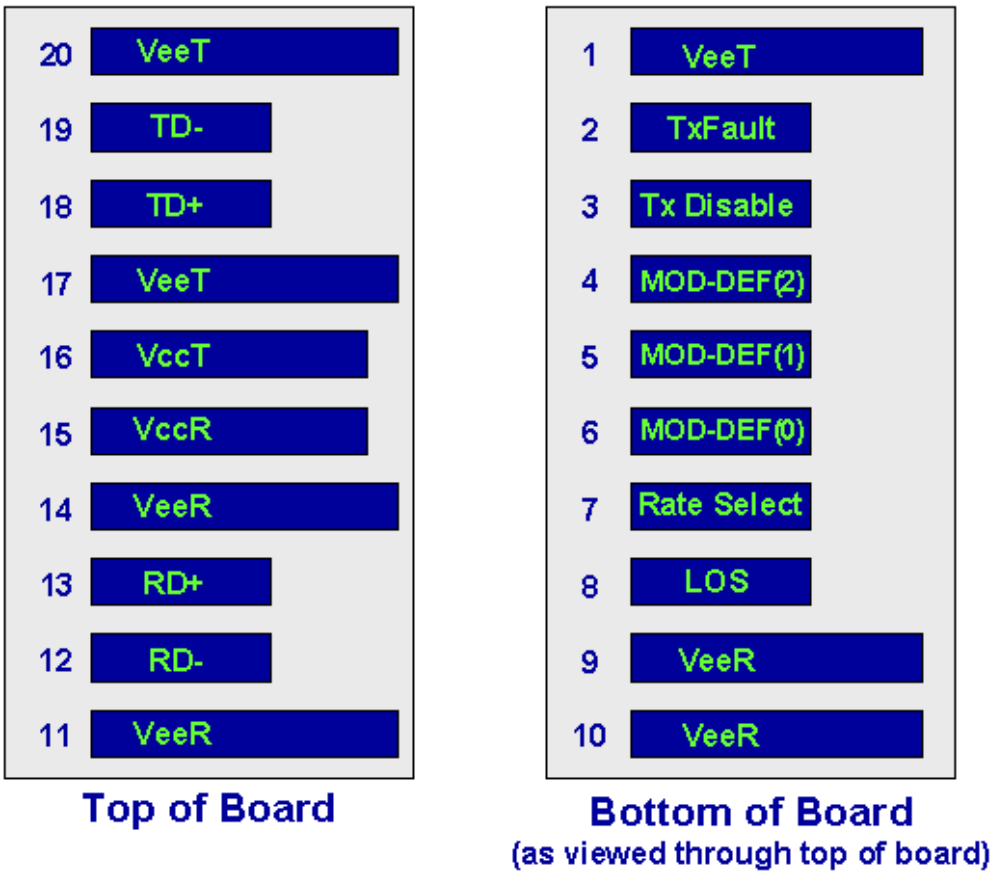

Figure 4-2 100Base-TX SFP Host Board Connector and related pin assignment

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4.2.1.1 Mating of SFP Transceiver PCB to SFP Electrical Connector

The 100Base-TX SFP transceiver shall be physically introduced into a host cage, which is mounted onto the housing motherboard. The layout of the connector, depicted in **Figure 4-3**, will insure the correct power up sequence of the 100Base-TX SFP.

- Pins 1, 9, 10 ,11, 14, 17 and 20 will engage first.
- Pins 15 and 16 will engage second.
- Pins 2, 3, 4, 5, 6, 7, 8, 12, 13, 18 and 19 will engage last.

The plating of the contacts of the 100Base-TX SFP transceiver PCB shall be as specified below:

- Contact area: 0.76 µm minimum hard gold over 2.54-µm minimum thick nickel.

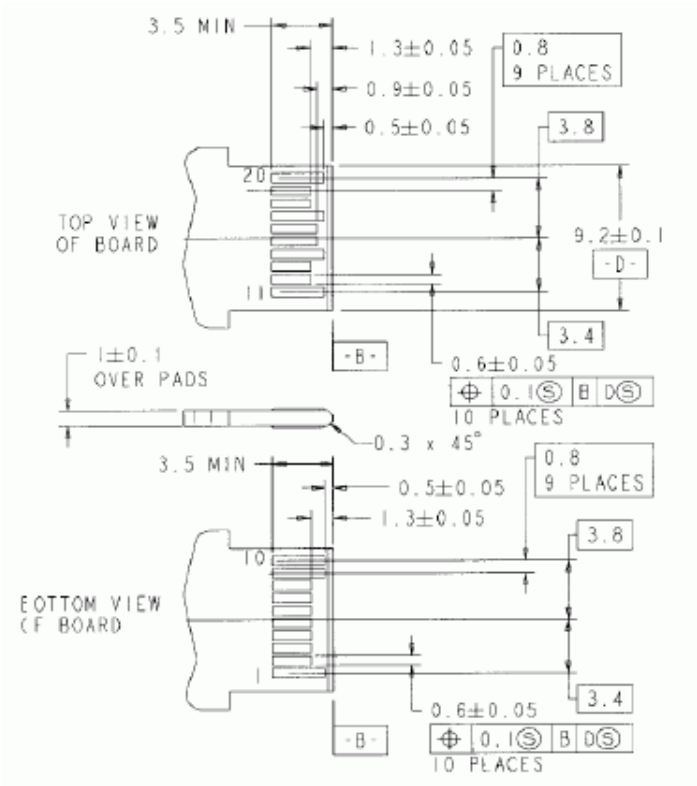

Figure 4-3 Pattern layout for 100Base-TX SFP PCB

End of section

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5 ELECROMAGNETIC COMPATIBILITY AND IMMUNITY

The 100Base-TX SFP must be capable of meeting the requirements detailed in this section when installed into the host equipment.

5.1 TELECOMMUNICATION SPECIFIC EMC TEST REQUIREMENTS

The 100Base-TX SFP Module shall meet the requirements of the following specifications:

FCC Chapter 47 Part 15, Sub-Part B, Section 15.109

6 SAFTY AND RELIABILITY

6.1 RELIABILITY

- Service life (operation within the required conditions, see Table 3-2 for details) > 15 years
- FIT Rate, referenced on t_{amb} = 65°C, CL = 60%, Ea = 0.8eV < 150 Fit

7 DEVICE PACKAGING AND MARKINGS

Each 100Base-TX SFP will be in bulk packaging per drawing MD0102 unless otherwise requested with specific agreement.

The 100Base-TX SFP transceiver shall also contain the following markings on a label:

- Part number.
- Serial number.

8 REFERENCES

[1] *Small Form Factor Pluggable Transceiver MultiSource Agreement (MSA)*, Sep 14, 2000;
[2] IEEE 802.3z, *Carrier Sense Multiple Access with Collision Detection Access Method and Physical Layer Specification*, 2002, Standard

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